REMARKS

Claims 3-4, 15-16, and 27-28 have been cancelled and claims 30-44 have been added; thus, claims 1, 5, 13, 17, 25, and 29-44 are all the claims pending in the application. Claims 1, 3-5, 13, 15-17, 25, and 27-29 stand rejected on prior art grounds; and, claims 3-4, 13, 15-16, and 27-28 stand objected to. Applicants respectfully traverse these rejections based on the following discussion.

I. The Claim Objections

Claims 3-4, 15-16, and 27-28 are objected to because the Office Action asserts that the claims are duplicated to the further limitation of their independent claims. Applicants have amended the claims, above, to cancel claims 3-4, 15-16, and 27-28.

Claim 13 is objected to because the Office Action asserts that appropriate correction is required to change "a cell having a guard ring" to "a cell having said guard ring". Applicants have amended claim 13, above, to replace "a" with "said". In view of the foregoing, the Examiner is respectfully requested to reconsider the objections to the claims.

II. The Prior Art Rejections

Claims 1, 3-5, 13, 15-17, 25, and 27-29 stand rejected under 35 U.S.C. §102(e) as being anticipated by Becker (U.S. Patent No. 6,550,047). Applicants respectfully traverse these rejections based on the following discussion.

The claimed invention provides a method of displaying a guard ring within an integrated circuit design having logic devices, wherein the logic devices and the guard ring symbolically

displayed in a single display. In the rejection, the Office Action argues that Becker teaches displaying logic devices and a guard ring graphically, semantically, or symbolically in a single display. In addition, the Office Action argues that Becker teaches displaying parameters, including at least one of a type of circuit, a type of guard ring, and an efficiency of the guard ring. However, nothing within Becker teaches displaying or otherwise showing the guard ring(s) or logic devices in a display. Applicants submit that nothing within Becker mentions displaying or otherwise showing anything in a display other than the selection table 150, which merely includes variables/characteristics that determine the size of an I/O cell. Moreover, the selection table 150 does not include parameters including the type of circuit, the type of guard ring, or the efficiency of the guard ring. Therefore, as explained in greater detail below, Applicants respectfully submit that the prior art of record does not teach or suggest the claimed invention.

The Office Action argues that Becker teaches displaying logic devices and a guard ring graphically, semantically, or symbolically in a single display (Office Action, pg.3, middle of pg.). In support for this contention, the Office Action cites column 4, lines 40-67 of Becker, which discloses displaying a selection table 150. More specifically, the Office Action asserts that if generated I/O cells are not to the designer's liking, the I/O cells can be regenerated after modifications to the design parameters by way of a design user interface display (Becker, col. 4, lines 51-54). Moreover, FIG. 1B provides a selection table 150 that includes a plurality of variables that are configured to determine the size of the I/O cell 108 for a particular design (Becker, col. 4, lines 59-62). The selection table 150 can be a text or graphical display having any layout, which prompts the user to provide information regarding each of the desired characteristics.

However, the selection table 150 does not display logic devices or a guard ring. Rather, the selection table 150 merely includes variables/characteristics that determine the size of an I/O cell.

The Office Action argues that FIGS. 3-4, column 7, lines 15-67, and column 8, lines 1-7 of Becker discloses the use of guard rings. Specifically, FIGS. 3-4 illustrate a generated I/O cell 108'. The Office Action asserts that P-tap guard ring slices 306a, P-tap guard ring corners 304a, P-tap guard ring slices 302, and ring slices 308 define a P-tap guard ring 402 (Becker, col. 7, lines 42-44). In a like manner, an N-tap guard ring 404 is defined within the ring slices 308, N-tap guard ring slices 306b, and N-tap guard ring corners 404b (Becker, col. 7, lines 49-52). Additionally, guard ring slices 308a include N-tap guard ring strips 406 and P-tap guard ring strips 408 (Becker, col. 7, lines 59-61).

However, nothing within Becker teaches displaying or otherwise showing the guard ring(s) or logic devices in a display. Applicants submit that nothing within Becker mentions displaying or otherwise showing anything in a display other than the selection table 150.

Conversely, as discussed in paragraph 0021 of Applicants' disclosure, a method displays a guard ring within an integrated circuit design by determining positions of the logic devices within the integrated circuit design, incorporating the guard ring into the integrated circuit design, and displaying the logic devices and the guard ring either graphically, semantically, or symbolically in a single display.

Furthermore, as discussed in paragraphs 0038 – 0040 of Applicants' disclosure, contrary to conventional systems that do not display or verify guard rings in semiconductor designs, embodiments of the invention provide verification, checking, and circuit simulation to determine

guard ring efficiency and latchup robustness. Thus, the invention provides intra- and inter-cell latchup parasitic information for latchup evaluation. Moreover, embodiments of the invention provide representation for checking and verification of guard rings by having a graphical, schematic, and symbol representation. In this way, the system can visualize the presence of the guard ring, see the guard ring in the schematic representation and have the guard ring contained in the symbol function.

Applicants submit that nothing within Becker teaches representing guard ring(s) in a display for checking and verifying the efficiency and latchup robustness of the guard ring(s). Rather, Becker merely teaches a *generated* I/O cell 108' comprising guard rings. Moreover, Becker discloses a display for a selection table 150; however, the selection table 150 does not display the guard rings or logic devices.

Applicants further note that although the Office Action asserts that Becker discloses displaying the selection table 150 textually or graphically, Becker does not teach displaying the selection table 150 semantically or symbolically.

Therefore, it is Applicants' position that Becker does not teach the claimed feature of "displaying said logic devices and said guard ring symbolically in a single display" as defined by independent claims 1 and 25.

In addition, the Office Action asserts that Becker teaches displaying a parameterized symbol (Office Action, bottom of pg. 3 and middle of pg. 5). In support for this contention, the Office Action cites column 7, lines 15-67 and column 8, lines 1-7, which assertedly discloses guard ring structures. However, Applicants respectfully submit that the portions cited by the Office Action do not disclose a method wherein any integrated circuit components or symbols

are displayed. As discussed above, nothing within Becker mentions displaying or otherwise showing anything in a display other than the selection table 150. Therefore, it is Applicants' position that Becker fails to teach the claimed feature of "displaying a parameterized symbol" as defined by independent claims 1, 13, and 25.

Furthermore, the Office Action argues that Becker teaches displaying parameters, including at least one of a type of circuit, a type of said guard ring, and an efficiency of said guard ring (Office Action, bottom of pg. 3 – top of pg. 4, middle of pg. 5). In support for this contention, the Office Action cites FIGS. 3-4, and 6, column 7, lines 15-67, column 8, lines 1-67, and column 9, lines 1-48, which assertedly discloses N-type transistor slices, P-type transistor slices, N-tap and P-tap guard rings, N-tap and P-tap guard ring strips, and a corner guard ring. However, nothing within Becker, including the portions cited by the Office Action, teaches *displaying* the type of circuit, the type of guard ring, and the efficiency of the guard ring.

As discussed more fully above, the only thing that Becker displays is the selection table 150. The selection table 150 includes variables/characteristics that determine the size of an I/O cell. Specifically, FIG. 1B illustrates the selection table 150, which includes a plurality of variables (Becker, col. 4, lines 59-60). FIG. 1B provides that the selection table 150 includes a pad pitch parameter 152, a tolerance parameter 154, a drive strength parameter 156, an input level parameter 158, an input buffer style parameter 160, a slew rate parameter 162, a ring voltage parameter 164, a staggered or inline pad arrangement parameter 166, a bond pad top layer metal parameter 168, and a core voltage parameter 169 (Becker, col. 5, lines 2-8).

However, nothing with Becker discloses that the selection table 150 includes parameters comprising the type of circuit, the type of guard ring, or the efficiency of the guard ring.

Therefore, it is Applicants' position that Becker fails to teach the claimed feature of "displaying parameters, including a type of said guard ring" as defined by independent claims 1, 13, and 25. Additionally, Applicants submit that Becker fails to teach the claimed features of "displaying said parameters including a type of circuit" as defined by dependent claims 33, 36, and 42; "displaying said parameters including an efficiency of said guard ring" as defined by dependent claims 34, 37, and 43; and, "displaying said parameters including a type of circuit and an efficiency of said guard ring" as defined by dependent claims 35, 38, and 44.

The Office Action further argues that Becker discloses displaying a portion of an integrated circuit design as a cell having a guard ring within a hierarchical integrated circuit design (Office Action, top of pg. 5 (citing col. 4, lines 50-56 and 64-66; col. 5, lines 47-53)).

Once more, the Office Action relies on the argument that Becker discloses displaying the selection table 150 to assert that Becker teaches displaying an element of the claimed invention. As more fully discussed above, the selection table 150 displays variables/characteristics that determine the size of an I/O cell. However, the selection table 150 does not display a portion of an integrated circuit design as a cell having a guard ring within a hierarchical integrated circuit design.

As also discussed above, nothing within Becker mentions displaying anything other than the selection table 150, including displaying a portion of an integrated circuit design as a cell having a guard ring within a hierarchical integrated circuit design. Therefore, Applicants' respectfully submit that Becker fails to teach the claimed feature of "displaying said portion of said integrated circuit design as a cell having said guard ring within said hierarchical integrated circuit design" as defined by independent claim 13.

Therefore, it is Applicants' position that Becker does not teach many features defined by independent claims 1, 13, and 25 and that such claims are patentable over the prior art of record. Further, it is Applicants' position that dependent claims 5, 17, and 29-44 are similarly patentable, not only because of their dependency from a patentable independent claims, but also because of the additional features of the invention they defined. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw the rejections.

II. Formal Matters and Conclusion

With respect to the rejections to the claims, the claims have been amended, above, to overcome these rejections. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw the rejections to the claims.

In view of the foregoing, Applicants submit that claims 1, 5, 13, 17, 25, and 29-44, all the claims presently pending in the application, are patentably distinct from the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to

discuss any other changes deemed necessary. Please charge any deficiencies and credit any overpayments to Attorney's Deposit Account Number 09-0456.

Respectfully submitted,

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